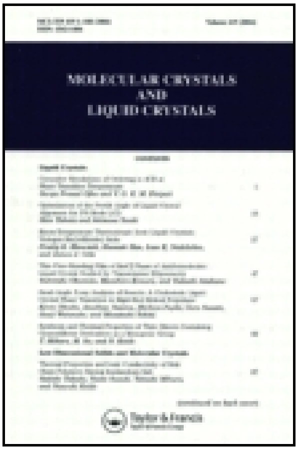

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High information content liquid crystal displays (minimum 250×250 picture elements) operated in the fast update (TV) mode require the incorporation of an electronic switch into each picture element. α-Si:H(F)[1] is a suitable material for the implementation of both two (diode) and three (TFT) terminal devices for matrix addressed LCDs. A simple analysis of α-Si TFTs shows that the low mobility of α-Si is an optimal match to the I_{off} requirements, while competing technologies (CdSe, poly-Si) encounter difficulties. However, using 10μ channel lengths, the mobility of α-Si was considered insufficient to drive active matrix displays. We report an innovative α-Si TFT which achieves short channel length and high mobility. The DC and the transient response characteristics will be presented. Ring oscillators were designed using this characteristic. Computer simulations suggest that an eleven stage ring oscillator utilizing α-Si TFTs can operate at 2.2 MHz. These advances will allow us to overcome the limitations in device response which has thus far prevented α-Si from being used in driving and addressing active matrix displays.

INTRODUCTION

Large flat-panel displays are being investigated today for applications in both computer terminals and flat-screen televisions. In particular, liquid crystal displays (LCDs) appear to be an ideal choice for low power applications.[2] Also, the technology exists today to make such displays on 12″×12″ inexpensive glass substrates. Three separate methods of driving LCDs have been utilized including (1) multiplexing,[3] (2) diode drivers,[4,5] and (3) thin film transistor (TFT) drivers.[6,7] TFTs have been investigated in a number of technologies such as CdSe,[8] microcrystalline silicon, polysilicon,[9] and amorphous silicon[10] (α-Si). In all of these materials except α-Si, the TFTs have difficulty reaching the extremely low off currents required for LCDs.

Microcrystalline and polycrystalline silicon have been investigated extensively for possible use in large-area displays.[9] It is believed that those materials may be the long-term choice for high-speed thin-film transistors, but at present, they are not applicable because of their numerous problems: (1) the deposition area is too small for large area displays; (2) the off-current values of TFTs, fabricated in the high-mobility materials is too large; (3) the process temperature is too high during deposition to be compatible with large-area display production; (4) the production of the high-mobility laser recrystallized α-Si materials does not seem feasible over large areas; or (5) the mobility achieved is still not large enough to insure high-speed TFTs capable of driving large area LCDs.

Nonetheless, if one is interested in active matrix drivers for high-density LCDs with at least 512×512 pixels, one needs a high-speed TFT switch to operate the display in the fast-update TV mode. This is the area where TFTs are most important as it is hoped that they will be used not only as the switch at each pixel element, but also as the on-substrate drivers. The incorporation of drivers directly onto the substrate with the display elements will greatly reduce the external circuitry required to drive the display in the TV mode and therefore will reduce the cost dramatically.

An example of the type of on-substrate circuitry required for a LCD is shown in Figure 1. If one is driving a 512-column by 512-row display in the fast update TV mode, then 512 rows must be addressed every 33.3 msec. This implies that one has approximately 65 μsec to address an individual row in the display. If the scheme in Figure 1 is utilized, then one must be able to shift 512 bits of information into the shift register in the allotted 65 μsec/row. This implies a propagation delay of 0.12 μsec/bit. If one assumes that there are three transistor propagation delays per flip flop in the shift register and latch, then the transistors must have no less than a 24 MHz cut-off frequency.

This frequency level could be achieved with 10 μm source-to-drain spacing TFTs only if the mobility was in the range of 50–100 cm^2/Vsec and if the parasitic capacitance of the device was minimized. This high mobility is not achievable in α-Si materials at present. There has been progress in α-Si growth processes and gate dielectric deposition techniques which have resulted in improved mobility values. Field-effect mobility values ranging from 0.1 to 0.3 cm^2/Vsec are typically found,[6] although a value of 1.9 cm^2/Vsec has been reported.[11] It is believed that the field-effect mobilities being achieved

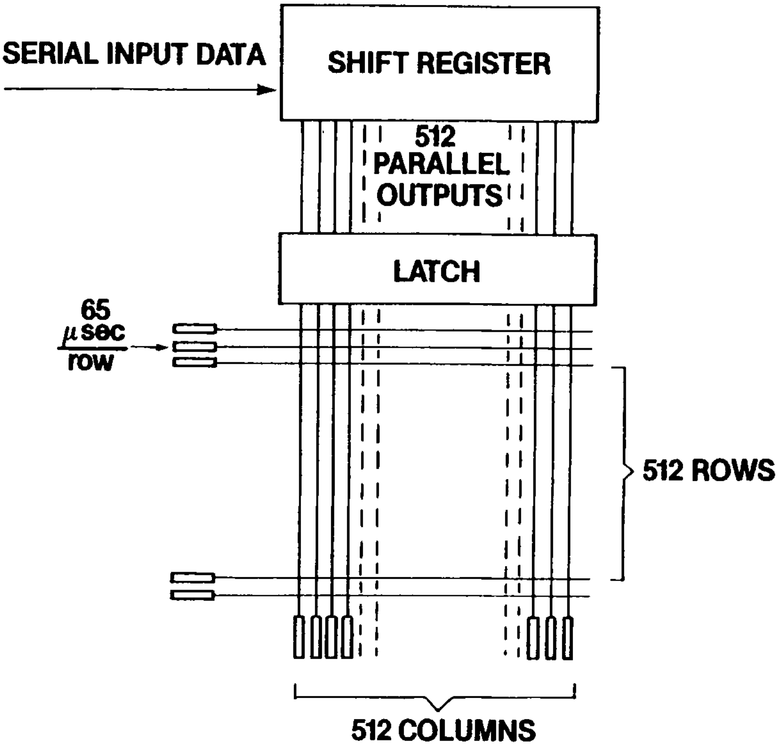

FIGURE 1 An example of the type of on-substrate circuitry required to drive a LCD in the TV mode. The shift register and latch can be built and operated at sufficient speeds if one uses the α-Si TFTs discussed in this paper.

today are close to the best that are possible in α-Si materials. Consequently, research to improve field-effect mobilities is unlikely to provide major gains in TFT frequency response. However, improvements in TFT frequency response can be quite dramatic if one reduces the gate length in a device because increases in frequency proportional to the inverse square of the gate length are possible. Thus, a reduction of gate length from 10 μm to 1 μm can result in a factor of 100 increase in TFT frequency of operation provided the transconductance increases and the gate capacitance decreases as the gate length is reduced. Thus, one must reduce the gate length in order to obtain an α-Si TFT which can be operated at a 24 MHz frequency. In this paper, we will discuss a new α-Si TFT with a 1-μm channel length which shows promise of approaching the cut-off frequency required to do on-display drivers.

METHODS AND RESULTS

In an attempt to fabricate a short channel length TFT, many new structures and fabrication sequences were tried.[12] We evaluated many of these structures from the viewpoint of channel length and reduced parasitic capacitance. One successful TFT structure will be discussed here.[13] Many other structures and what we believe is the ultimate α-Si TFT structure will be the discussion of future publications.[14]

One way to make short channel length TFTs is shown schematically in Figure 2. The structure is based on the vertical-flow concept rather than the more conventional horizontal flow. This allows one to make 1 μm TFTs without the need for critical lithography. The channel lengths are essentially defined by the thicknesses of the materials and in the case of the TFT shown in Figure 2, by the angle of the reactive-ion etching step employed to define the beveled edge. The process sequence for the short-channel TFT is also shown in Figure 2. Note that no less than 10-μm photolithography is used throughout the processing.

Results from a typical TFT are shown in Figure 3. The results shown are for a device with a 150-μm gate width, 1-μm gate length,

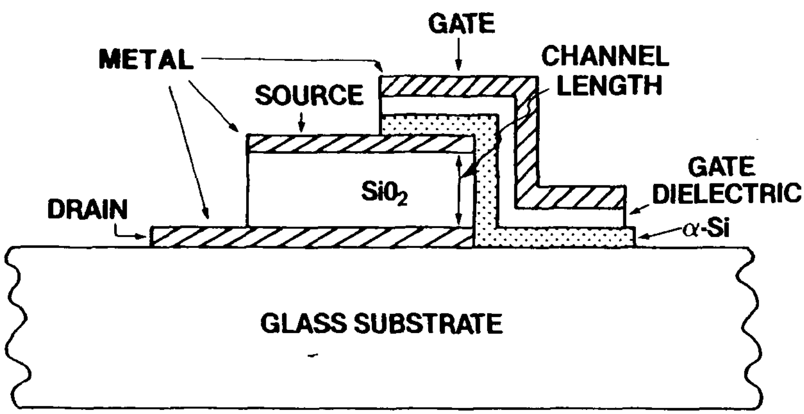

FIGURE 2 A cut-away representation of a vertical-flow α-Si TFT. Note that the channel length is defined by the thicknesses of the deposited materials and by the angle of the reactive-ion etching step employed to define the beveled edge.
Process Sequence:
1. Deposit metal, SiO_2 and metal.
2. Mask for the RIE step.
3. Etch away the metal, SiO_2, and metal to the substrate surface.
4. Deposit α-Si, SiO_2 gate dielectric, and metal gate.
5. Define the gate using 10-μm photolithography.
6. Open up a contract to the drain.

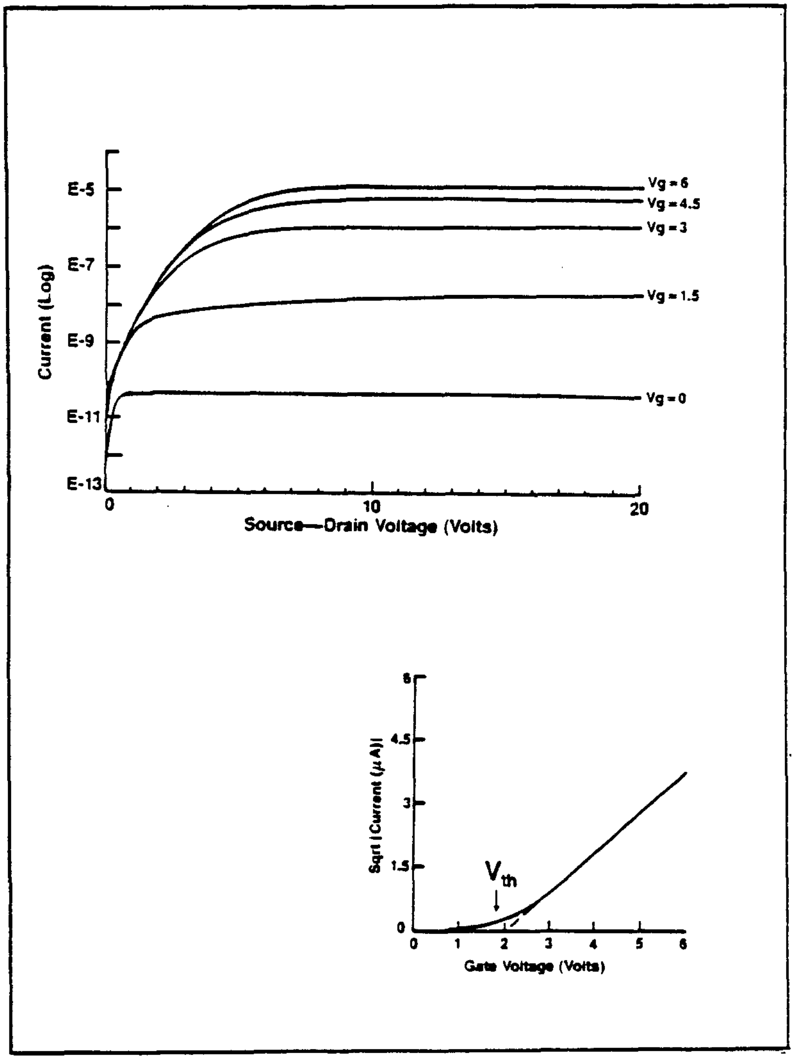

FIGURE 3a Current voltage characteristics for the 1 μm channel length α-Si TFT.

FIGURE 3b Square root of the source-drain current vs. gate voltage for source drain voltage equal to 10 volts.

0.3-μm α-Si thickness, 0.3-μm SiO_2 gate dielectric thickness, and a 0.8-μm SiO_2 separation layer between the source and drain. As can be determined from Figure 3, the threshold voltage was 1.9 V and the field-effect mobility was 1.0 cm^2/Vsec.

The excellent current capabilities of the short-channel TFT seem ideally suited for both switches and drivers for large flat-panel displays. An analysis of a TFT-based ring oscillator has been conducted. The approach taken was to analyze a single-stage inverter with a capacitive load. Then a computer simulation was performed where many inverter stages were cascaded together to arrive at an estimate of the delay between successive stages in a ring oscillator.[15] The delay between alternate stages, 2Δ, represents one rise time and one fall time in a ring oscillator. Therefore, the frequency of operation may be calculated from

$$f = \frac{1}{n(2\Delta)}, \tag{1}$$

where n is the number of stages in the ring oscillator.

The analysis was based upon the circuit of Figure 4. Here, V_{dd} is the power supply voltage, V_i is the input voltage, V_o is the output voltage and C is the capacitance at the output node of the inverter stage. A MOSFET model was used for the α-Si TFT.[6]

In order to understand the ring-oscillator and to formulate a set of design rules to achieve high-frequency ring-oscillator performance, a computer analysis was performed. A simulation of numerous cascaded inverters ($i = 1$ to m) was carried out where the input to the first inverter was a step, and the output of inverter i became the input to inverter $i + 1$, and so on for a structure of m stages. After approximately ten inversions, every other waveform produced by inversion looked essentially the same, but delayed in time. Considering the nth stage, then the output voltage $V_n(t) = V_{n+2}(t-2\Delta)$ where 2Δ is a constant time delay, $2\Delta = t_{\text{rise}} + t_{\text{fall}}$.

Many parameter values were inserted into the computer analysis to model a TFT ring oscillator and to isolate trends in the design rules which would be beneficial to high-speed operation.[16] These trends are summarized in Table I. In Table I, β is the ratio of the driver width to the load width in an inverter stage (the gate length is the same for all transistors in the vertical flow configuration). In particular, one set of values being $C = 0.15$ pF, $V_{th} = 2$ V, $V_{dd} = 15$ V, $\beta = 3$, $K_D = 2.88 \times 10^{-6}\ A/V^2$, $K_L = 9.6 \times 10^{-7}\ A/V^2$, and $\mu = 1$ cm^2/Vsec was inserted, which for an oxide thickness of 0.3 μm

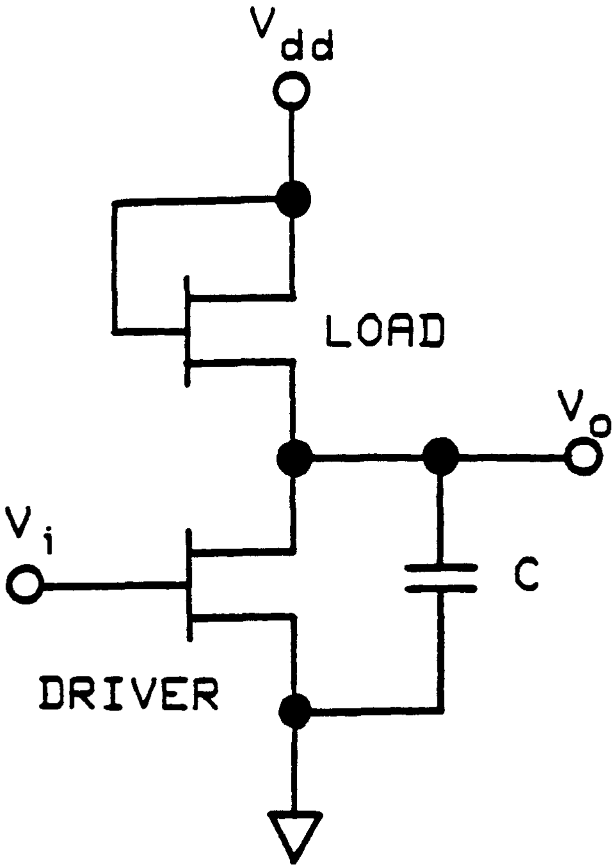

FIGURE 4 Circuit diagram of a single stage inverter used in the analysis of a ring oscillator.

produced $f_{T\,\max} \simeq 2.22$ MHz. K_D and K_L used above, are device constants for the driver and load respectively.[15]

A variation of parameters was performed which led to the conclusions of Table I. The results of this computer analysis are shown in Figure 5, indicating the relationship between Δ, the average inverter stage-delay time, and the four parameters C, β, V_{th} and V_{dd}. While these parameters are not totally independent of each other, the choice of an optimum set should be possible.

As we have already mentioned, a load capacitance of 0.15 pF will be difficult to achieve, but it is not theoretically impossible. The analysis of a ring-oscillator in a small signal model predicts the node

TABLE I

Design rules for TFT ring oscillators.

Parameter being controlled	Change necessary to increase ring-oscillator frequency
C	Decrease
V_{th}	Decrease
β	Decrease
V_{dd}	Increase
μ	Increase

capacitance between two inverter stages is[17]

$$C = C_{gd}^{L} + C_{ds}^{L} + C_{ds}^{D} + C_{gs}^{D} + 2(1+A)C_{gd}^{D} \tag{2}$$

where C_{gd}^{L} is the gate-drain capacitance of the load, C_{ds}^{L} and C_{ds}^{D} are the drain-source capacitances of the load and driver, respectively, C_{gs}^{D} is the gate-source capacitance of the driver, and $2C(1+A)C_{gd}^{D}$ is twice the Miller capacitance, $C_{\text{Miller}} = (1+A)C_{gd}^{D}$, between the gate and drain of the driver. A is the magnitude of the gain in the inverter stage. The Miller capacitance is counted twice since the gate-drain

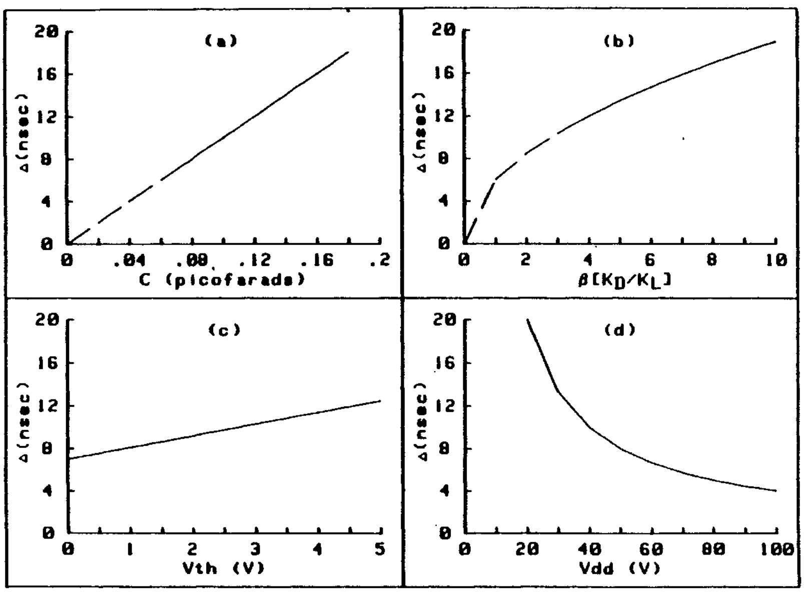

FIGURE 5 Relationship between stage delay time and various TFT design parameters: a) Δ vs. C; b) Δ vs. β; c) Δ vs. V_{th}; and d) Δ vs. V_{dd}.

capacitance transitions are from a state where it is charged to a "1" on the gate with a "0" on the drain to the state where a "0" is on the gate and a "1" is on the drain. Thus, the charge changes on the gate-drain capacitor by $Q = 2 \cdot C_{\text{Miller}} \cdot V_{dd}$.

We believe that the vertical structures for TFTs can provide a load capacitance for each inverter stage of only 0.15 pF.[16] This relatively low capacitance value when combined with the current-voltage characteristics shown in Figure 3 suggests that ring oscillators could operate at about 2–5 MHz. This result is very encouraging since it is close to the frequency required to put α-Si TFT drivers on the same substrate with a LCD pixel.

CONCLUSION

We have been able to make 1-μm channel length TFTs which promise to allow clocking at low-megahertz rates. This is a very important step toward the incorporation of α-Si TFT drivers on the same substrate with the LCD pixels. Our efforts in this area are continuing toward larger circuits with short-channel TFTs. We expect in the near future to have displays with both switches and drivers operating on the same substrate. The success of large active-matrix displays will hinge on the achievements being made presently with short-channel TFTs.

Acknowledgment

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